Digital Logic Design Practical's (CS302P)

Assignment # 01

Fall 2025

Total marks = 20

Deadline

22nd of November 2026

Please carefully read the following instructions before attempting the assignment.

RULES FOR MARKING

It should be clear that your assignment would not get any credit if:

- The assignment is submitted after the due date.
- The submitted assignment does not open, or the file is corrupted.
- Strict action will be taken if the submitted solution is copied from any other student or the internet.

You should consult the recommended books to clarify your concepts, as handouts are insufficient.

You are supposed to submit your assignment in Doc or Docx format.

Any other formats like scanned images, PDF, ZIP, RAR, PPT, BMP, etc. will not be accepted.

Topic Covered:

The objective of this assignment is to assess the understanding of students about:

- Lab Work - Week # 03 - Digital logic circuits analysis and converting Boolean expressions to digital circuits
- Lab Work - Week # 04 - Boolean Algebra and Simplification of Boolean Expressions
- Lab Work - Week # 05 - DE Morgan's Theory and the Universal Gates

Topic Covered

Lab Experiment # 01 to Lab Experiment # 05

NOTE

No assignment will be accepted *via email after the due date* (whether it is due to load shedding, internet malfunctioning, etc.). Hence, refrain from uploading assignments within the last hour of the deadline. It is recommended that the solution be uploaded at least two days before its closing date.

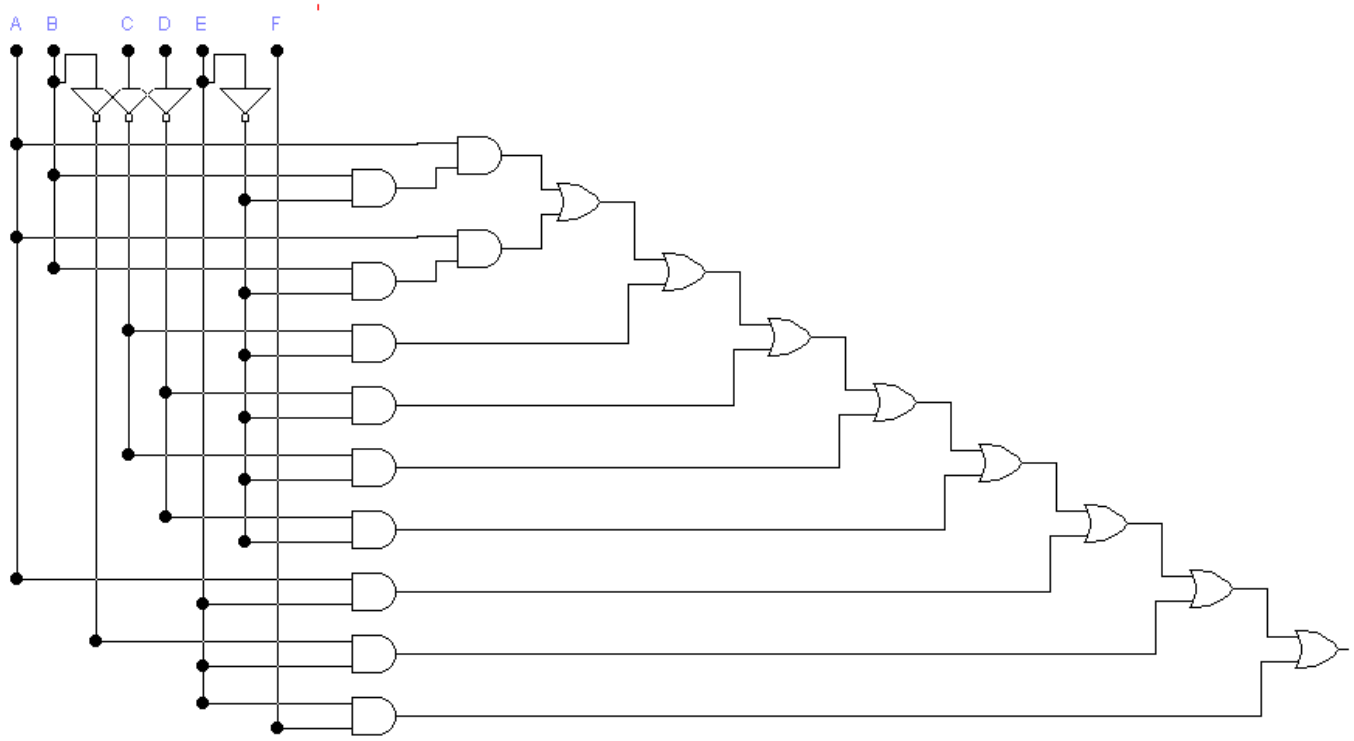
If you find any mistakes or confusion in the assignment (Question statement), please consult your instructor before the deadline. After the deadline, no queries will be entertained in this regard.

For any query, feel free to email me at:

CS302P@vu.edu.pk

Question No 01 **Marks (20)**

You are provided a circuit diagram, which is designed from a Boolean Expression having Six (06) variables. Your task is to draw the same circuit in Electronics Workbench and then, using a Logic Converter, simplify the circuit and share the **simplified Boolean Expression** along with NAND-based gate level diagram.



Note: You must have to enter your Student ID as a label of Last Gate or Output. Type your Equations and Paste your images in MS Word (doc or docx) file to submit. Any other files like PDF or Separate Images will not be accepted and awarded ZERO marks.